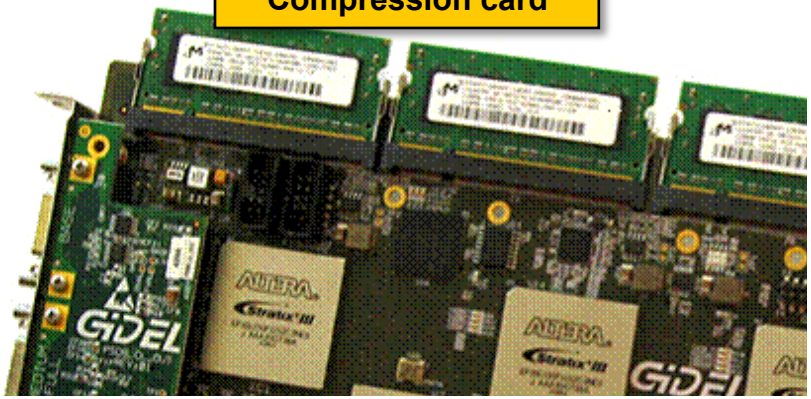
Dr. Eric J. Balster
Embedded Data Processing Laboratory (EDPL)

Dr. Balster's research focuses on processing of large scale imagery for real-time computation. This type of processing includes: compression, enhancement, mosaic generation, and registration of imagery. Typically, the processing of such large imagery requires the use of acceleration cards for parallel computation and faster throughput. Much of the work involved with using these types of cards requires translation from a software implementation to a hardware description language (HDL) implementation of such algorithms.

EDPLs JPEG2000 Compression card



EDPLs Large-Scale Persistent Surveillance System

Large-Scale Imaging of the Dayton Area

Reconfigurable Computing Projects (Balster, Scarpino)

- VTC acceleration with FPGAs (2000)
- Rapid Prototyping System (RPS) (2004)
- P-Frame simplification (2005) *Predator transition*
- JPEG2000 compression (2005)
  - JPIP image communication protocol (2007) *AF transition*
  - FPGA compression acceleration (2008) *AF transition*
  - FPGA decompression acceleration(2009) *AF transition*
- DREAM board development (2006) *AFRL/RY transition*
- Mixed Signal Design Workbench (2008)
- Non-linear Equalization of A/D converters (2009)
- A/D converter, mixed signal modeling and sim. (2009)