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Method for Fabricating Thin film Structures with Negative Inductance

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Detailed Description of the Invention

Method for Fabricating Thin film Structures with Negative Inductance

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I. INTRODUCTION

Literature shows quite a number of works being done on the subject of negative inductance. However, almost none of them explain how to actually create one without using synthesized circuits where active components are used for the controller to reproduce the behavior of negative inductance. Synthesized circuits work as intended and are fine for macro sized electronic circuits where space and complexity may not be an issue. In microelectronic circuits however, where space is precious, those methods are not desirable. Thus there is a need to find better ways to create negative inductance, and it will be ideal if the negative inductance itself can be realized as a single passive component just like regular resistor, capacitor, or inductor.

II. INDUCTOR FABRICATION

To create the inductor, aluminum and copper are alternately deposited using RF plasma sputtering system. Figure 1 illustrates the micro inductor fabrication steps.

The process is started with the deposition of SiO_2 on silicon wafer to provide electrical isolation. The deposition is done by RF plasma sputtering with crystal monitor to achieve thickness of 1000\AA . The next step is applying LOR on top of the SiO_2 . LOR is necessary to provide “under cut” for the lift-off process, a process that removes photoresist and any deposition on it to reveal the desired pattern on the silicon wafer. LOR10B is applied by spin coating at 2000 rpm to get a thickness of approximately 12500\AA . Soft baking at 180C for 5 minutes completes the LOR application.

SPR955, a positive type photoresist, is then spin coated at 3000rpm to get a thickness of approximately 10000Å. Soft baking at 100C for 90 seconds completes the SPR955 application.

The next step is ultra violet exposure to transfer the micro inductor pattern onto the photoresist followed by developing it in MF319 for about 1 minute. Figure 2 is a cross section image taken with SEM to show the undercut after developing in MF319.

Aluminum and copper are then deposited alternately onto the wafer by RF plasma sputtering method with thickness ratio of Al:Cu = 1334Å:666Å, these layers are repeated five times to get a total thickness of 1um. Figure 3 is a cross section SEM image showing the alternating layers of aluminum and copper.

The lift-off process is done by placing the sputtered wafer in EBR solution. Figure 4 shows the final micro inductor structures. It is a ten turn circle spiral with 100um track width, 100um spacing, and 200um inner radius.

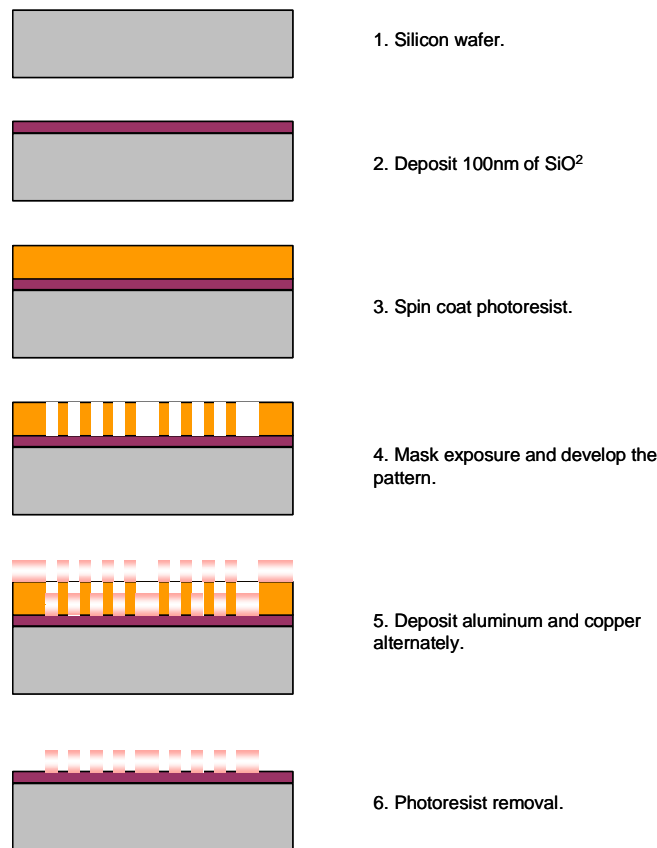


Fig. 1. Micro inductor fabrication steps.

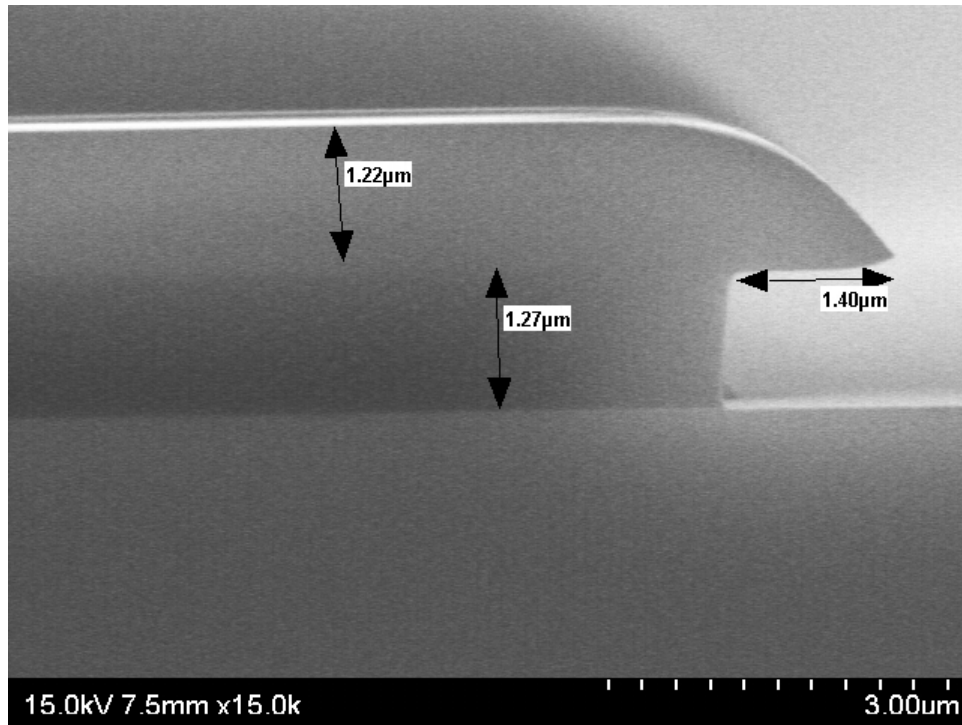


Fig. 2. LOR undercut.

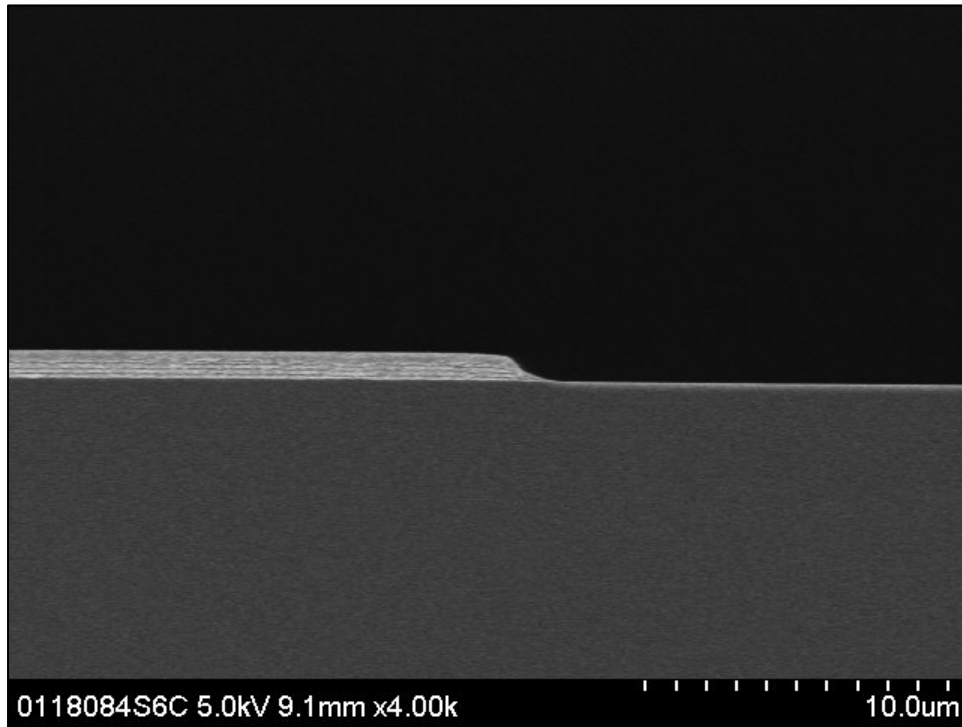


Fig. 3. Alternating layers of Al and Cu.



Fig. 4. Spiral micro inductor.

III. MEASUREMENT

To measure the inductance, HP85046A S-Parameter Test Set and HP8753C Network Analyzer are used. Full 2-ports measurements are taken and the results are in S-parameters, thus a conversion is needed to calculate the final inductance value. Equations (1) – (3) describe the inductance calculation from S-parameters.

$$\Delta_S = (1 + S_{11})(1 + S_{22}) - S_{12}S_{21} \quad (1)$$

$$Y_{21} = \frac{-2S_{21}}{\Delta_S} \quad (2)$$

$$\text{Inductance} = \frac{-im(\frac{1}{Y_{21}})}{2\pi f} \quad (3)$$

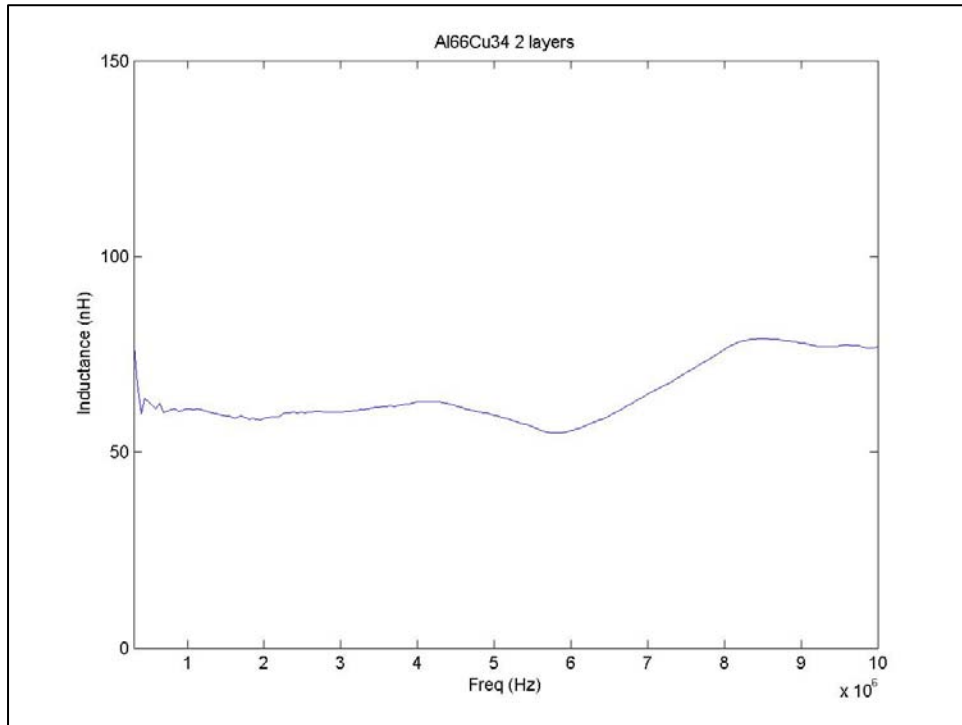


Fig. 5. Inductance of only 2 layers of Al and Cu.

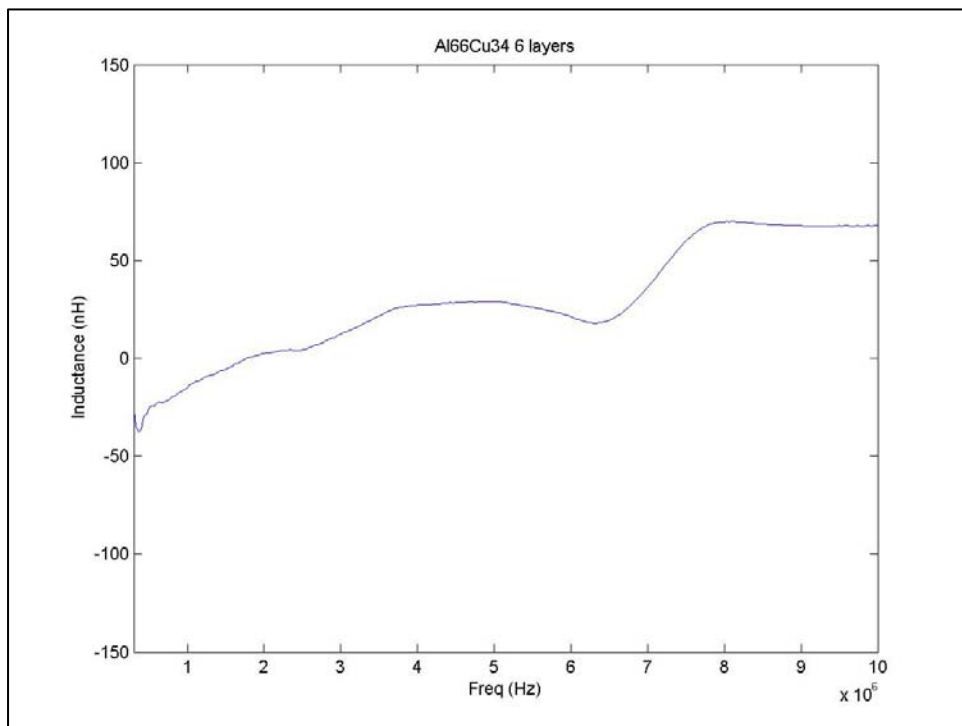


Fig. 6. Inductance of 6 layers of Al and Cu.

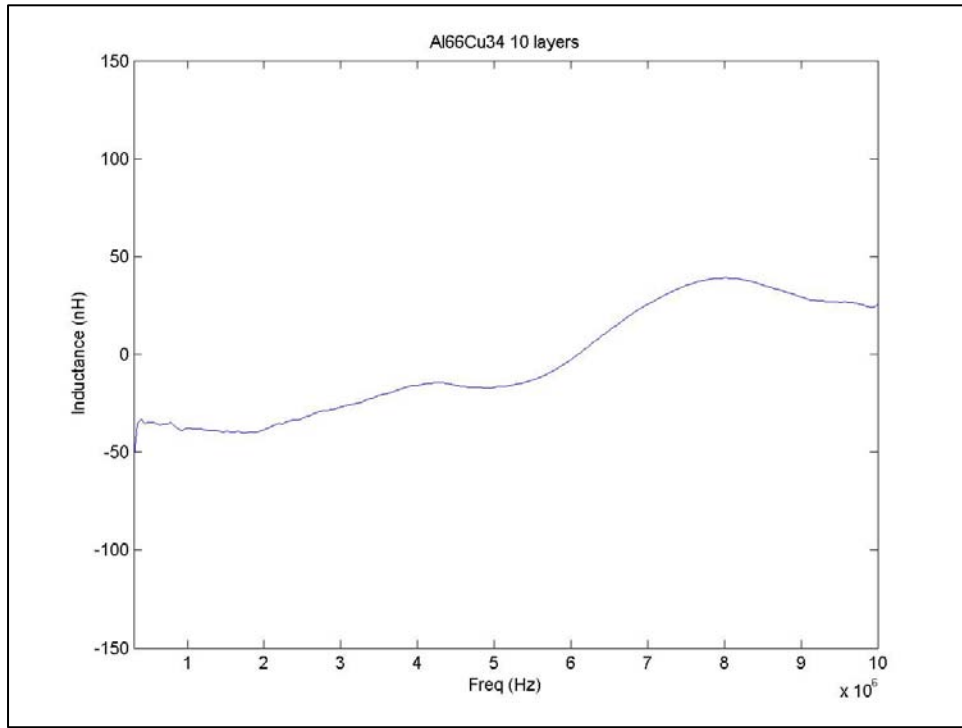


Fig. 7. Inductance of 10 layers of Al and Cu.

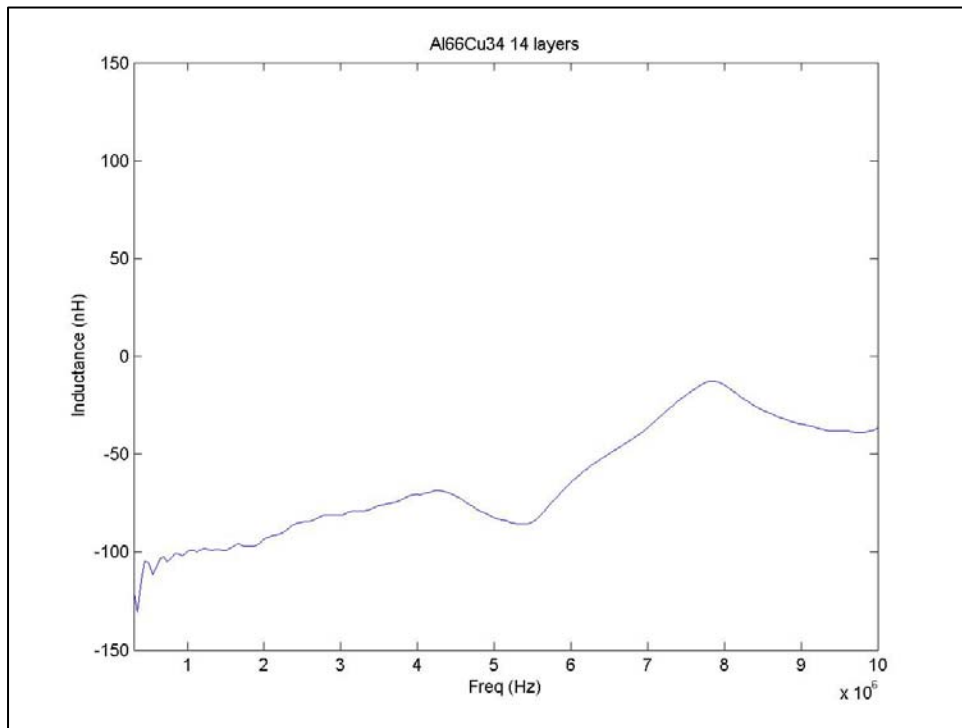


Fig. 8. Inductance of 14 layers of Al and Cu.

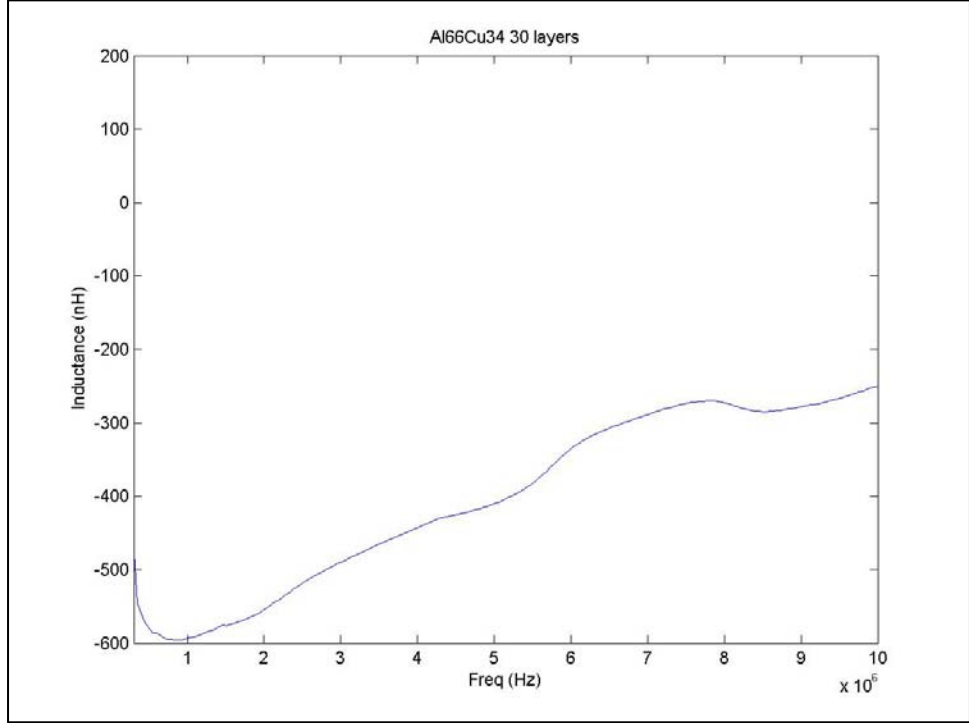


Fig. 9. Inductance of 30 layers of Al and Cu.

The trend that is shown in Figure 5-9 strongly indicates a connection between the number of layers and negative inductances. The more layers being used, maintaining the same bulk thickness, the more negative the inductance that is generated. This relation is still being investigated further at the moment this paper is written.

IV. TEST AND VERIFICATION

A test has been performed to verify the negative inductance functionality in an actual circuit. The purpose of the test is to demonstrate a condition where unwanted parasitic inductance being compensated with the negative inductance. To setup the test a micro inductor with positive inductance is fabricated and connected in series by wire bonding it with another micro inductor having negative inductance. Figure 10 shows the setup and Figure 11 shows the test result.

The test result confirms that the negative inductance indeed compensates the parasitic inductance in series connection having $L_{total} = L_{parasitic} + L_{negative}$.

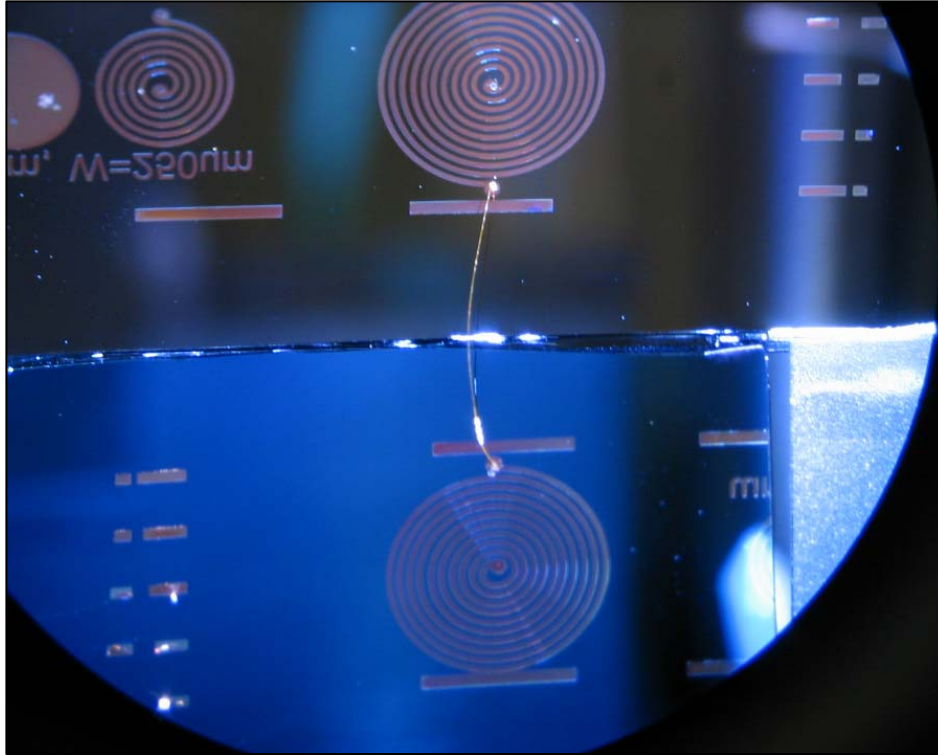


Fig. 10. Positive inductance in series with negative inductance.

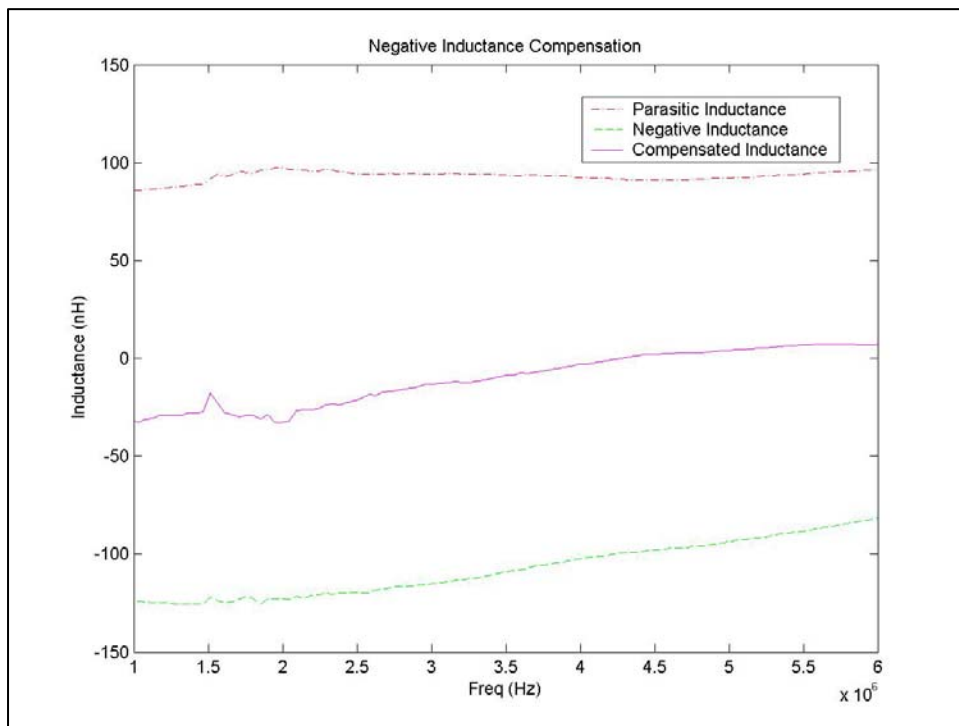


Fig. 11. Inductance compensation test result.

V. CONCLUSION

The intention of this invention is to realize negative inductance as one truly passive component that so far can only be synthesized or simulated using more complex electronic circuits. A method for fabricating negative micro inductor has been introduced, actual devices have been fabricated and tested. Copper and aluminum were used for this experiment, however this method should not be limited to copper and aluminum only, other materials can also be used.

The applications of this invention is very broad, however we can already see a bright future in high speed digital VLSI (Very Large Scale Integrated Circuit) design where parasitic inductances are becoming a big issue for signal integrity. Some other applications are for voltage regulation, displacement factor correction for maximum power factor, optoelectronics, compensation of transmission lines, and antenna bandwidth enhancement. General application will be for inductance compensation in any electronic circuits that suffer from unwanted inductances.

VI. INVENTORS' ROLE

Agus Widjaja: Inventor, person who performs all experiments and measurements.

Andrew Sarangan: Technical advisor, laboratory and equipments provider.